UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/576,767	05/24/2000	Yung-Soo Kim	030681-200	4658

21839 7590 05/21/2004

BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
RYMAN, DANIEL J	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/576,767	KIM ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20 and 24-29* is/are allowed.

6)☒ Claim(s) *1,4,8,11,15,16 and 21* is/are rejected.

7)☒ Claim(s) *2,3,5-7,9,10,12-14,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Although Applicant has amended the abstract in order to overcome the objection to the Specification, the Abstract still exceeds 150 words. Therefore, the objection to the Specification remains.

2. Applicant's arguments filed 5/3/2004 have been fully considered but they are not persuasive. On pages 27-28, Applicant argues that Cimini does not point out how the apparatus of Cimini meets the steps of (b), (c), and (d) in claim 1 and the limitation recited in claim 8, lines 3-8. Examiner, respectfully, disagrees; however, Examiner will further elaborate on the teachings of Cimini. Claim 1 step (b) calls for "forming a block of N coded data and dividing the block into L M-sized small blocks, where N, M, and L indicate integers of 1 or more and L=N/M" and claim 8, lines 3-8 calls for a "transmission deinterleaver" that performs this step. Cimini discloses taking a serial data stream and breaking it into N symbol segments in ref. 119 (forming a block of N coded data where ref. 119 is, as broadly defined, a "transmission deinterleaver"). These N symbol blocks are then converted into a parallel stream in ref. 31 (dividing the block into L M-sized small blocks where L is the number of parallel streams the block is divided into and M is the size of each parallel stream). Given a broad reading, Examiner maintains that Cimini teaches the limitations of claim 1, step (b) and claim 8, lines 3-8

3. Step (c) of claim 1 calls for "M-point inverse fast Fourier transforming the L small blocks" and claim 8, lines 3-8 calls for a device to perform this step. Cimini discloses that the parallel signals (L small blocks) are passed through a FFT unit (ref. 41). It is implicitly disclosed that this FFT unit is an IFFT unit. Cimini discloses that the signal output from the FFT unit is

eventually modulated using a time domain signal (ref. 52), which provides evidence that the signal output from the FFT is a time domain signal. Having a time domain signal output from an FFT unit can only occur if the FFT unit is an IFFT unit. In addition, as Applicant acknowledges (see specification: page 1, line 20-page 2, line 10), it is well known in the art to use an IFFT to change a symbol sequence into a sequence which can be transmitted (time-domain sequence). Thus, Examiner maintains that Cimini teaches the limitations of claim 1, step (c) and claim 8, lines 3-8.

4. Claim 1, step (d) requires "combining L M-point inverse fast Fourier transformed blocks, and generating an N-sized inversely-transformed block". Cimini teaches combining the L parallel signals in a parallel-to-serial converter into an N-sized inversely-transformed serial block. As such, as broadly defined, Examiner maintains that Cimini teaches the limitations of claim 1, step (d).

5. On pages 28-29, Applicant argues that the combination of Cimini and Daffara does not teach the limitation of claim 4 and 11 since Cimini does not teach the limitations of the claimed invention as discussed above. Examiner maintains that Cimini does teach the limitations of the claimed invention, given the above arguments. As such, Examiner maintains that Cimini and Daffara teach, or at the very least suggest, the limitations of claims 4 and 11.

6. On pages 29-31, Applicant argues, with respect to claims 15 and 21, that Cimini does not show "a pre-processor for encoding an input data sequence and converting the encoded data to parallel data". Examiner, respectfully, disagrees. Cimini discloses an encoder (ref. 21) and a serial-to-parallel converter (ref. 26). As broadly defined, the combination of the encoder and serial-to-parallel converter can be viewed as a "pre-processor". As such, Examiner maintains that

Cimini discloses "a pre-processor for encoding an input data sequence and converting the encoded data to parallel data".

7. Applicant further argues that Cimini does not disclose "a block signal domain transformer..., and combining time domain signals". Again, Examiner, respectfully, disagrees. Cimini discloses an S/P converter (ref. 31). This S/P converter, as broadly defined, divides the encoded data into blocks of predetermined sizes. Cimini also discloses an FFT unit (ref. 41), which given the above arguments, is an IFFT device wherein the FFT unit changes the domain of the signals from the frequency domain to the time domain. Finally, Cimini discloses a P/S converter (ref. 45) which combines the parallel time-domain signals into a single serial time-domain signal. Taken together, as broadly defined, these elements comprise a "block signal domain transformer". Thus, Examiner maintains that Cimini discloses "a block signal domain transformer for dividing the encoded data into blocks of predetermined sized, transforming each block into a time-domain signal, and combining time domain signals".

8. Applicant goes on to argue that Cimini does not disclose "a pilot signal adder for coverting pilot tones, which are to be inserted at positions other than a predetermined position among the positions at which '0' has been inserted in the block domain transformer, into time time domain pilot signals, and adding the pilot signals to the time domain signals output by the block signal domain transformer" since Cimini does not disclose where the pilot tones are added to the signal or that the pilot tones are used for the same reason as Applicant's claimed invention. Examiner, respectfully, disagrees. In the rejection, Examiner equates the inserted "0" with a guard band. Cimini discloses that the pilot signals are added in addition to the guard band (col. 4, lines 40-50; col. 5, line 56-col. 6, line 8; and col. 7, line 65-col. 8, line 14). Thus, Cimini

suggests that the pilot signals are added in addition to the inserted "0". Therefore, Examiner maintains that Cimini discloses the "pilot signal adder" where the pilot signal is inserted in a location distinct from the location of the inserted "0".

9. In addition, Applicant argues that Cimini does not disclose "a pilot signal adder" since Cimini does not teach that the pilot tones are used for the same reason as Applicant's claimed invention. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the pilot tones are used for the same reason as Applicant's claimed invention) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). If Applicant determines that the reason the pilot tones are used is an important feature then Applicant should claim such features.

10. Applicant additionally argues that Cimini does not teach "a post-processor for converting the resultant signals of the pilot signal adder to serial signals". Examiner, respectfully, disagrees. Cimini discloses that a pilot tone is added to the output from the block signal transformer (cluster) (col. 4, lines 40-50 and col. 7, line 65-col. 8, line 14). Cimini also discloses that the signal input to the D/A converter is a serial signal (col. 4, lines 51-56). Thus, Examiner maintains that Cimini discloses, or at the very least suggests, converting the signal containing the blocks and the pilot tones into a serial signal.

11. Furthermore, Applicant argues that it would not have been obvious to modify Cimini to insert "0" at the first position of each block since Applicant inserts "0" in order to avoid DC offset in contrast to Examiner's position that the "0" could be used as a guard interval. Applicant

argues that adding a guard interval is done in order to avoid intersymbol interference where Applicant has added the cyclic prefix in order to avoid intersymbol interference. Therefore, Applicant argues that "the guard interval of Cimini et al. is not the same as inserting '0s' as recited in the claims". Examiner, respectfully, disagrees. Examiner notes that the features upon which applicant relies (i.e., the cyclic prefix is used for preventing intersymbol interference and the "0s" are inserted to avoid DC offset) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Examiner submits that Cimini discloses inserting a guard interval in addition to a cyclic prefix (col. 5, line 56-col. 8, line 8). Therefore, since Applicant does not specify for what the cyclic prefix and the "0s" are used, Examiner maintains that Cimini reads on the language of the claims.

12. Given the above arguments, Examiner maintains the rejection of the claims. Examiner urges Applicant to amend the claims in order to add limitations to the claims which will distinguish the claims from the prior art. Applicant repeatedly argues that Cimini does not recite limitations of the invention where the limitations are not in the claims. These aforementioned limitations could be added to the claims in order to distinguish the claims from the prior art.

Drawings

13. The drawings are objected to because "M-IFFT" on page 14, line 13 of the specification appears as "N-IFFT" in Fig. 6. In addition, "M-FFT" on page 17, line 6 of the specification appears as "N-FFT" in Fig. 16.

Specification

14. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

16. Claims 1 and 8 are rejected under 35 U.S.C. 102(a) as being anticipated by Cimini et al (USPN 5,914,933).

17. Regarding claims 1 and 8, Cimini discloses a method and apparatus for transmitting orthogonal frequency division multiplexing (OFDM) signals, the method comprising the steps of and the apparatus comprising means for: coding the OFDM signals (ref. 21 and col. 2, line 63-col. 3, line 17); forming a block of N coded data (ref. 119; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56) and dividing the block into L M-sized small blocks, where N, M and L indicate integers of 1 or more, and L = N/M (ref. 31; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); M-point inverse fast Fourier transforming the L small blocks (ref. 41; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); combining L M-point inverse fast Fourier transformed blocks, and generating an N-sized inversely-transformed block (ref. 45; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); attaching a cyclic prefix to the N-sized inversely-transformed block (col. 5, line 56-col. 6, line 8); and transforming the blocks having the attached cyclic prefix, into an analog signal (ref. 47; col. 2, line 63-col. 3, line 17; and

col. 3, line 44-col. 4, line 56) and transmitting the transformed analog signal (ref. 60; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cimini et al (USPN 5,914,933) in view of Daffara et al (USPN 5,687,165).

20. Regarding claims 4 and 11, Cimini discloses a method and apparatus for transmitting orthogonal frequency division multiplexing (OFDM) signals, the method comprising the steps of and the apparatus comprising means for: coding the OFDM signals (ref. 21 and col. 2, line 63-col. 3, line 17); forming a block of N coded data (ref. 119; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56) and dividing the block into L M-sized small blocks, where N, M and L indicate integers of 1 or more, and L = N/M (ref. 31; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); M-point inverse fast Fourier transforming the L small blocks (ref. 41; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); combining L M-point inverse fast Fourier transformed blocks, and generating an N-sized inversely-transformed block (ref. 45; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); attaching a cyclic prefix to the N-sized inversely-transformed block (col. 5, line 56-col. 6, line 8); transforming the blocks having the attached cyclic prefix, into an analog signal (ref. 47; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56) and transmitting the transformed analog signal (ref. 60; col. 2, line

63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); and when receiving the signal, digitally converting received OFDM signals and obtaining a signal sample from the transformed signals (ref. 68 and col. 7, line 41-64) and detecting the starting point of an N-sized signal sample block from the signal samples (col. 7, line 41-64). Cimini does not expressly disclose a method and apparatus for receiving orthogonal frequency division multiplexing (OFDM) signals, the method comprising the steps of and the apparatus comprising means for: removing a cyclic prefix; dividing the signal sample block into L M-sized small blocks, where N, M and L are integers of 1 or more, and L = N/M; M-point fast Fourier transforming the L small blocks; combining the L M-point fast Fourier transformed small blocks, and generating an N-sized transform block; and detecting data from the N-sized transform block, and decoding the detected data. Instead, Cimini discloses, as a non-limiting example of a receiver, that, since clustering only applies at the receiver, can be implemented without explicitly performing the reverse of the clustering process (col. 7, line 35-64). However, it is well known in the art to perform the reverse process in the receiver as was performed in the transmitter in order to obtain the original signal, as is evidenced by Daffara (Fig. 4; col. 3, lines 24-25; and col. 3, line 37-col. 4, line 8). It would have been obvious to one of ordinary skill in the art at the time of the invention to perform the reverse process in the receiver as was performed in the transmitter in order to obtain the original signal, as is well-known in the art.

21. Claims 15, 16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cimini et al (USPN 5,914,933).

22. Regarding claims 15 and 21, Cimini discloses a method and apparatus for transmitting orthogonal frequency division multiplexing (OFDM) signals, the method comprising the steps of

and the apparatus comprising means for: encoding an input data sequence (ref. 21 and col. 2, line 63-col. 3, line 17), and converting encoded data to parallel data (ref. 119; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); dividing the encoded data into blocks of predetermined sizes (ref. 119 and ref. 31; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); transforming each block to a time domain signal (ref. 41; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56), and combining the time domain signals (ref. 45; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); transforming pilot tones, which are to be inserted at positions, into time domain pilot signals (col. 4, lines 40-50 and col. 7, line 65-col. 8, line 14), and adding each of the pilot signals to the time domain signal of each block (col. 4, lines 40-50 and col. 7, line 65-col. 8, line 14); and converting the resultant signal of the transforming step to a serial signal (ref. 45; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56), adding a cyclic prefix to the converted signal (col. 5, line 56-col. 6, line 8), converting the resultant signal to an analog signal (ref. 47; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56), and transmitting the analog signal (ref. 60; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56). Cimini does not expressly disclose inserting "0" at the first position of each block after dividing the encoded data into blocks of predetermined sizes; however, Cimini does disclose adding a guard interval between the blocks (col. 5, line 56-col. 6, line 8), where it is implicit that a guard band placed on the start of the block would place the guard band between blocks. It is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57

USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Cimini discloses the use of a guard interval, any value for the interval, including "0", would have been obvious, absent a showing of criticality by applicant.

23. Regarding claim 16, referring to claim 15, Cimini discloses that the block signal domain transformer comprises: a transmission deinterleaver for dividing the encoded data into L M-sized blocks (ref. 31; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); a "0" inserter for inserting "0" at the first position of each block (col. 5, line 56-col. 6, line 8), an Lx(M-IFFT) for performing inverse fast Fourier transformation on each block (ref. 41; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); and a transmission interleaver for combining the time domain signals with each other (ref. 45; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56).

Allowable Subject Matter

24. Claims 2 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method disclosed for dividing and combining blocks is not expressly disclosed in the prior art.

25. Claims 3 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method disclosed for dividing and combining blocks is not expressly disclosed in the prior art.

26. Claims 5 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method disclosed for dividing and combining blocks is not expressly disclosed in the prior art.

27. Claims 6 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method disclosed for dividing and combining blocks is not expressly disclosed in the prior art.

28. Claims 7 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not fairly suggest fast Fourier transforming the signal, equalizing the signal, and inverse fast Fourier transforming the signal (equalizing the signal in the frequency domain) before dividing the signal into blocks, and then fast Fourier transforming the blocks (processing the signal).

29. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method disclosed for dividing and combining blocks is not expressly disclosed in the prior art.

30. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method disclosed for dividing and combining blocks is not expressly disclosed in the prior art.

31. Claims 17-20 and 24-29 are allowed. The prior art did not fairly suggest, in a receiver, inserting a virtual pilot tone at predetermined positions of a received frequency domain signal; extracting the virtual pilot tone in addition to pilot tones added upon transmission; and using the virtual pilot tone and the pilot tones added upon transmission to estimate channel characteristics.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (703)305-6970. The examiner can normally be reached on Mon.-Fri. 7:00-5:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703)308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel J. Ryman
Examiner
Art Unit 2665

DJR

Daniel J. Ryman

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600